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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,765	12/16/2003	Ram Huggahalli	P17381	5720

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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,765	HUGGAHALLI ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
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6/12/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 21 have been examined.

Response to Arguments

2. Applicant's arguments filed 21 April 2006 have been fully considered but they are not persuasive.

3. In Applicants arguments to claims 1 – 14, and 18 – 21, applicant states that the relied upon reference, US Patent Application Publication No. 2004/0128450 (hereinafter Edirisooriya), does not teach or suggest that a processor (Edirisooriya; Figure 1 Items 12a, 12b, and 12c) may arrange for information to be routed to a different processor (Remarks; Page 10 Lines 9 – 10). However, Applicant does state that "non-processor agent" (Edirisooriya; Figure 1 Items 20a or 20b) may push information directly into processor caches (Edirisooriya; Figure 1 Items 14a, 14b, and 14c) (Remarks; Page 10 Lines 7 – 9). Applicant also states that determining which processor is to receive the information is performed at the non-processor agents (Remarks; Page 10 Footnote [1]).

4. The Examiner respectfully disagrees with the argument presented by the Applicant. It appears that Applicant has interpreted the processors (Edirisooriya; Figure 1 Items 12a, 12b, and 12c) as both the requesting agent processor and the target processor. However, the Examiner has interpreted the processors (Edirisooriya; Figure 1 Items 12a, 12b, and 12c) as the target processors and the "non-processor" agents (Edirisooriya; Figure 1 Items 20a and 20b) as the requesting agent processor. "Non-processor" agent is described in Edirisooriya as "input/output controllers and direct

memory access devices" (Edirisooriya; Paragraph [0002] Lines 1 – 4). Controllers are known in the art as processors that are designed and programmed to perform a specific function. "Non-processor" agents determine to send data to a target processor cache (Remarks; Page 10 Footnote [1]) and the "non-processor" agent is different than the target processor.

5. In Applicants arguments to claims 15 – 17, Applicant argues that Edirisooriya does not teach that the destination be associated with a system memory for one type of I/O traffic and with a processor cache for another type of I/O traffic (Remarks; Page 10 Lines 17 – 23).

6. The Examiner has determined that the limitation listed above is not a necessary requirement of claim 15. The term "may" suggests that the limitation does not have to be present in the current invention, but could be present. The use of the term "may" makes the claim indefinite because it is not clear if the limitation is required or not.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 15 – 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 15, the claim recites the limitation "wherein the destination ***may*** be associated with a system memory for one type of I/O traffic and with a processor cache for another type of I/O traffic" (emphasis added). The recitation of "may" makes the claim indefinite because it is not clear if the limitation is a part of the claim or not. The term "may" suggests that the limitation does not have to be present in the current invention, but could be present. Therefore, the limitation has not been treated further.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 – 5, and 7 – 21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication No. 2004/0128450 (hereinafter Edirisooriya).

As per claims 1, 12, 18, and 20, Edirisooriya teaches determining at a requesting agent processor (Edirisooriya; Figure 1 Items 20a and 20b) that Input Output (I/O) traffic is to be received at a target processor cache (Figure 1 Items 14a, 14b, and 14c), wherein the target processor is different than the requesting agent processor; receiving from the requesting agent routing information associated with I/O traffic (Figure 2 Item

22); and arranging for the I/O traffic to be transferred directly into the target processors cache in accordance with the routing information (Figure 2 Item 28, Paragraphs [0019] – [0020]).

As per claims 2, 13, 16, 19, and 21, Edirisooriya inherently teaches wherein the routing information is received from an I/O driver executing at the requesting agent because the device (Figures 1 and 4 Items 20a and 20b) sends the push request to the processors (Figure 1 Items 12a – 12c, Figure 4 Items 12d – 12f) and data transfers between computer system CPUs and I/O devices are inherently performed by I/O drivers.

As per claims 3, 14, and 17, Edirisooriya teaches wherein the routing information includes a target processor identifier (Paragraph [0019]).

As per claim 4, Edirisooriya teaches wherein the I/O traffic is associated with a network or a network interface controller (Figure 1 Items 20a, and 20b, Paragraphs [0013] – [0014], and [0030]).

As per claim 5, Edirisooriya teaches wherein the arranging is performed in multi-processor system (Figure 1 Items 12a, 12b, and 12c) that includes a plurality of potential targets (Figure 1 Items 14a, 14b, and 14c, Paragraph [0012]).

As per claim 7, Edirisooriya teaches wherein the I/O traffic includes information packets (Paragraph [0033]).

As per claim 8, Edirisooriya teaches wherein the method further comprises receiving the I/O traffic (Paragraph [0033]); and determining whether the I/O traffic should be transferred directly into the target processors cache (Paragraphs [0033] and [0034]).

As per claim 9, Edirisooriya teaches wherein the routing information indicates that one type of I/O traffic should be transferred directly into the target processor cache while another type of I/O traffic should be transferred directly into another target processor cache (Paragraphs [0032] – [0034]).

As per claim 10, Edirisooriya teaches wherein the I/O traffic is received from a peripheral device (Figures 1 Item 21, Paragraphs [0013] and [0014]).

As per claim 11, Edirisooriya inherently teaches wherein the I/O traffic is transferred into the target processors cache in accordance with a chipset's routing function because the interconnection network (Figure 1 Item 16, Figure 4 Item 72) inherently routes data to the processors (Figure 1 Items 12a – 12c) in accordance with its routing function (Figure 4 "PUSH").

As per claim 15, Edirisooriya teaches an input path (Figure 4 "PUSH") to receive from a requesting agent processor (Figure 4 Items 20a and 20b) routing information associated with Input Output (I/O) traffic (Figure 2 Item 22); and a processing element to arrange for the I/O traffic to be transferred directly into a destination (Figure 4 Item 14e) in accordance with the routing information (Figure 2 Item 28, Paragraphs [0019] – [0020]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edirisooriya et al. US Patent Application Publication No. 2004/0128450 (hereinafter Edirisooriya) as applied to claims 1 – 5, and 7 – 21 above in view of US Patent No. 6,574,682 (hereinafter Chan).

As per claim 6, Edirisooriya teaches the method as described per claim 1 (see rejection of claim 1 above).

Edirisooriya does not *explicitly* teach wherein the arranging is performed by at least one of a direct memory access (DMA) controller and an I/O controller hub.

However, Chan teaches wherein data is directly transferred to a cache using a DMA controller (Chan; Col 3 Lines 31 – 35, Col 4 Lines 1 – 8).

Therefore, it would have been obvious to one or ordinary skill in the art at the time the invention was made to have modified the teachings of Edirisooriya by that of Chan to include the data transfer through a DMA controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Edirisooriya by that of Chan because using a DMA controller allows for the data transfer to take place without the intervention of the processor associated with the cache, which increases system performance (Chan; Col 4 Lines 56 – 59).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Patent Examiner
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